

Gan, Kwang-Jow (甘廣宙)

Professor

■ **Educations**

- Ph.D., National Cheng Kung University, R.O.C. (1993-1997)
- M.S., National Cheng Kung University, R.O.C. (1989-1990)
- B.S., National Cheng Kung University, R.O.C. (1984-1988)

■ **Academic Focus**

- VLSI Engineering
- VLSI Design
- Nonlinear Circuit Design
- Semiconductor Physics and Devices
- Nano Devices and Thin Film
- Light Emitting Diode
- Electro-Optical Devices and Applications
- Energy-Saving Engineering

■ **Teaching Area**

- Engineering Mathematics
- Microelectronics
- VLSI Engineering
- VLSI Manufacturing
- Analog VLSI Design
- Semiconductor Physics and Devices
- Nano Science and Technology
- Electro-Optical Devices and Engineering

Publication

I. Refereed Papers

1. J.J. Lu, T.S. Mo, **K.J. Gan**, J.F. Chou, M.K. Lee, “Magnetic anomalies and spin-glass-like behavior in Ce₂CuGe₆”, **accepted by** Journal of Superconductivity and Novel Magnetism, March, 2011. (ISSN:0304-8853) (SCI)
2. **Kwang-Jow Gan***, Cher-Shiung Tsai, **Chi-Wen Hsien**, Yu-Kuang Li, and Wen-Kuan Yeh, “Design of Monostable-Bistable Transition Logic Element Using the BiCMOS-Based Negative Differential Resistance Circuit”, **revised by** **Analog Integrated Circuits and Signal Processing**, December, 2010.
3. **Kwang-Jow Gan***, Cher-Shiung Tsai, Yu-Kuang Li, “Design of Monostable-Bistable Transition Logic Element Using the BiCMOS-Based Negative Differential Resistance Circuit”, **revised by** **Analog Integrated Circuits and Signal Processing**, December, 2010. (ISSN:0925-1030) (SCI)
4. J. J. Lu, T. C. Lin, S. Y. Tsai, T. S. Mo, **K. J. Gan**, “Structural, magnetic and transport properties of Ni-doped ZnO films”, Journal of Magnetism and Magnetic Materials, Vol. 323, Iss. 6, pp. 829-832, March, 2011. (ISSN:0304-8853) (SCI)
5. Wen-Kuan Yeh, Yu-Ting Chen, Fon-Shan Huang, Chia-Wei Hsu, Chun-Yu Chen, Yean-Kuen Fang, **Kwang-Jow Gan**, and Po-Ying Chen, “The Improvement of High-k/Metal Gate pMOSFET Performance and Reliability using Optimism Si cap/SiGe Channel Structure”, **accepted by** **IEEE Transactions on Device and Materials Reliability**, August, 2010. (ISSN: 1530-4388) (SCI)
6. **Kwang-Jow Gan***, Cher-Shiung Tsai, Yu-Kuang Li, and Jeng-Jong Lu, “Logic Circuit Design Using Monostable-Bistable Transition Logic Element Based on Standard BiCMOS Process”, **Microelectronics Journal**, Vol. 42, No. 2, pp. 477-482, February, 2011. (ISSN:0026-2692) (SCI)
7. **Kwang-Jow Gan***, Cher-Shiung Tsai, Yan-Wun Chen, and Wen-Kuan Yeh, “Voltage-Controlled Multiple-Valued Logic Design Using Negative Differential Resistance Devices”, **Solid-State Electronics**, Vol. 54, Iss. 12, pp. 1637-1640, December, 2010. (ISSN:0038-1101) (SCI)
8. J. J. Lu, T. S. Mo, **K. J. Gan**, T. C. Lin, and M. K. Lee, “Observation of RKKY-Kondo Competition and Non-Fermi-Liquid Behavior in the Intermetallic

Compound Series $Ce(Cu_{1-x}Ni_x)Si_2$ ", **Journal of Superconductivity and Novel Magnetism**, Vol. 23, Iss. 8, pp. 1473-1477, June, 2010. (ISSN: 1557-1939) (SCI)

9. **Kwang-Jow Gan***, Dong-Shong Liang, and Yan-Wun Chen, "Novel Multiple-Valued Logic Design Using BiCMOS-Based Negative Differential Resistance Circuit Biased by Two Current Sources", **IEICE Transactions on Information & Systems**, Special Section on Multiple-Valued Logic and VLSI Computing, Vol. E93-D, No.8, pp. 2068-2072, August, 2010. (ISSN: 0916-8532) (SCI)
10. **Kwang-Jow Gan***, and Dong-Shong Liang, "Investigation of Adjustable Current-Voltage Characteristics and Hysteresis Phenomena for Multiple-Peak Negative Differential Resistance Circuit," **IEICE Transactions on Electronics**, Vol. E93-C No.4, pp.514-520, April, 2010. (ISSN: 0916-8524) (SCI)
11. **Kwang-Jow Gan***, Cher-Shiung Tsai, and Dong-Shong Liang, "Design and Characterization of the Negative Differential Resistance Circuits Using the CMOS and BiCMOS Process," **Analog Integrated Circuits and Signal Processing**, Vol. 62, No. 1, pp. 63-68, January, 2010. (ISSN:0925-1030) (SCI)
12. J.J. Lu, S.Y. Tsai, Y.M. Lu, T.C. Lin, and **K.J. Gan**, "Al-doping effect on structural, transport and optical properties of ZnO films by simultaneous RF and DC magnetron sputtering," **Solid State Communications**, Vol. 149, Iss. 47-48, pp. 2177-2180, December, 2009. (ISSN: 0038-1098) (SCI)
13. Dong-Shong Liang, **Kwang-Jow Gan***, Cheng-Chi Tai, and Cher-Shiung Tsai, "Standard BiCMOS Implementation of a Two-Peak Negative Differential Resistance Circuit with High and Adjustable Peak-to-Valley Current Ratio," **The Institute of Electronics, Information and Communication Engineers (IEICE) Transactions on Electronics**, Vol. E92-C, No. 5, pp. 635-638, May, 2009. (SCI) (ISSN: 0916-8524)
14. **Kwang-Jow Gan***, Dong-Shong Liang, and Cher-Shiung Tsai, "Novel Multiple-Selected and Multiple-Valued Memory Design Using Negative Differential Resistance Circuits Suitable for Standard SiGe-Based BiCMOS Process," **Analog Integrated Circuits and Signal Processing**, Vol. 59, Issue 2, pp. 161-167, May, 2009. (ISSN:0925-1030) (SCI)
15. **Kwang-Jow Gan***, Dong-Shong Liang, Cher-Shiung Tsai, Chun-Ming Wen, and Yaw-Hwang Chen, "Design and Fabrication of Multiple-Valued Multiplexer Using Negative Differential Resistance Circuits and Standard SiGe Process," **Solid State Electronics**, Vol. 52, No. 6, pp. 882-885, June, 2008. (ISSN:0038-1101) (SCI)

16. **Kwang-Jow Gan***, Cher-Shiung Tsai, Dong-Shong Liang, Chun-Da Tu, and Yaw-Hwang Chen, "Multiple-Input NOR Logic Design Using Negative Differential Resistance Circuits Implemented by Standard SiGe Process," **Solid State Electronics**, Vol. 52, Iss. 2, pp. 175-178, February, **2008**. (ISSN:0038-1101) (SCI)
17. **Kwang-Jow Gan***, Dong-Shong Liang, Cher-Shiung Tsai, Yaw-Hwang Chen and Chun-Ming Wen, "Multiple-Valued Decoder Using MOS-HBT-NDR Circuit," **Electronics Letters**, Vol. 43, No. 20, pp. 1092-1093, September, **2007**. (ISSN: 0013-5194) (SCI)
18. **Kwang-Jow Gan***, Cher-Shiung Tsai, and Wei-Lun Sun, "Fabrication and Application of MOS-HBT-NDR Circuit Using Standard SiGe Process," **Electronics Letters**, Vol. 43, No. 9, pp. 516-517, April, **2007**. (ISSN: 0013-5194) (SCI)
19. **Kwang-Jow Gan***, Cher-Shiung Tsai, Dong-Shong Liang, Chun-Ming Wen, and Yaw-Hwang Chen, "Tri-Valued Memory Circuit Using MOS-BJT-NDR Circuits Fabricated by Standard SiGe Process," **Japanese Journal of Applied Physics**, Vol. 45, No. 46, pp. L977-979, **2006**. (ISSN: 0021-4922) (SCI)
20. **Kwang-Jow Gan***, Yaw-Hwang Chen, Cher-Shiung Tsai, and Long-Xian Su, "Four-Valued Memory Circuit Using Three-Peak MOS-NDR Devices and Circuits," **Electronics Letters**, Vol. 42, Iss. 9, pp. 514-515, **2006**. (SCI)
21. **Kwang-Jow Gan***, "Investigation of the Combined Current-Voltage Characteristics of Two Similar Esaki-Diode-Like Devices," **Japanese Journal of Applied Physics**, Vol. 42, No. 10, pp. 6354-6358, **2003**. (SCI)
22. **Kwang-Jow Gan*** "Characterization of the extrinsic hysteresis phenomena of series-connected identical Esaki-diode-like NDR devices," **Japanese Journal of Applied Physics**, Vol. 41, No. 3A, pp. 1293-1299, **2002**. (SCI)
23. **Kwang-Jow Gan*** "The low-high-low I-V characteristics of five to seven peaks based on four NDR devices," **IEEE Transactions on Electron Devices**, Vol. 48, No. 8, pp. 1683-1687, **2001**. (SCI)
24. **Kwang-Jow Gan*** "Hysteresis phenomena for the series circuit of two identical negative differential resistance devices," **Japanese Journal of Applied Physics**, Vol. 40, No. 4A, pp. 2159-2164, **2001**. (SCI)
25. **Kwang-Jow Gan*** "Novel four-peak or five-peak current-voltage characteristics for three negative differential resistance devices in series," **Solid State Electronics**, Vol. 44, pp. 1597-1602, **2000**. (SCI)
26. **Kwang-Jow Gan*** and Yan-Kuin Su, "Novel multipeak current-voltage characteristic of series-connected negative differential resistance devices," **IEEE Electron Devices Letter**, Vol. 19, No. 4, pp. 109-111, **1998**. (SCI)

27. **Kwang-Jow Gan***, Yan-Kuin Su and Ruey-Lue Wang, "Simulation and analysis of negative differential resistance devices and circuits by load-line method and Pspice," **Solid State Electronics**, Vol. 42, No. 1, pp. 176-180, **1998. (SCI)**
28. **Kwang-Jow Gan*** and Yan-Kuin Su, "Modeling current-voltage and hysteretic current-voltage characteristics with two resonant tunneling diodes connected in series," **Solid State Electronics**, Vol. 41, No. 12, pp. 1917-1922, **1997. (SCI)**
29. **Kwang-Jow Gan*** and Yan-Kuin Su, "Modeling multipeak current-voltage characteristic and hysteresis phenomena for several resonant tunneling diodes connected in series," **Journal of Applied Physics**, Vol. 82, No. 11, pp. 5822-5828, **1997. (SCI)**
30. **Kwang-Jow Gan*** and Yan-Kuin Su, "Improved circuit design of multipeak current-voltage characteristics based on resonant tunneling diodes," **Japanese Journal of Applied Physics**, Vol. 36, No. 10, p.p. 6280-6284, **1997. (SCI)**
31. **Kwang-Jow Gan***, Yan-Kuin Su and Ruey-Lue Wang, "Modeling of three-peak current-voltage characteristics with two resonant tunneling diodes connected in series," **Journal of Applied Physics**, Vol. 81, No. 10, pp. 6825-6829, **1997. (SCI)**
32. Y. K. Su, F. S. Juang, N. Y. Li, **K. J. Gan** and T. S. Wu, "Heteroepitaxial growth of gallium antimonide on GaAs by low pressure MOVPE," **Solid State Electronics**, Vol. 34, No. 8, pp. 815-819, **1991. (SCI)**
33. Y. K. Su, **K. J. Gan***, F. S. Juang and J. S. Hwang, "Characterization of Si-implanted gallium antimonide," **Nuclear Instruments and Methods in Physics Research**, B55, pp. 794-797, **1991. (SCI)**
34. Y. K. Su, F. S. Juang, and **K. J. Gan**, "Ohmic contacts of AuGeNi and Ag/AuGeNi to n-GaSb with various sintering temperature," **Japanese Journal of Applied Physics**, Vol. 30, No. 5, pp.914-916, **1991. (SCI)**
35. Y. K. Su and **K. J. Gan***, "Raman spectra of Si-implanted GaSb," **Journal of Applied Physics**, Vol. 68, No. 11, pp.5584-5587, **1990. (SCI)**
36. F. S. Juang, Y. K. Su, N. Y. Li, and **K. J. Gan**, "Effects of TMSb/TEGa ratios on epilayer properties of GaSb grown by low pressure MOCVD," **Journal of Applied Physics**, Vol. 68, No. 12, pp.6383-6387, **1990. (SCI)**

II. International Conference (overseas)

1. **Kwang-Jow Gan***, Ping-Feng Wu, Wu-Yan Shie, Cher-Shiung Tsai, Dong-Shong Liang, Cheng-Hsiung Tsai, and Wen-Kuan Yeh, "Frequency Multiplier Design Using BiCMOS-Based Multiple-Peak NDR Circuit", 2010

IEEE International Conference on Electron Devices and Solid-State Circuits, Hong Kong, December 15-17, **2010**.

2. B.-J. Li, C.-H. Chang, Y.-K. Su, **K.-J. Gan**, and J.-W. Hong, "Thermal Dissipation of High Brightness Light Emitting Diode by using Multi-walled Carbon Nanotube/SiC Composites", 23rd International Microprocesses and Nanotechnology Conference, Fukuoka, Japan, Nov. 9-12, **2010**.
3. **Kwang-Jow Gan**, Kuan-Yu Chun, and Dong-Shong Liang, "Frequency Divider Design Using Λ -Type Negative Differential Resistance Circuit", IEEE International Midwest Symposium on Circuits and Systems, Seattle, Washington, USA, Aug. 1-4, **2010**, pp. 969-972.
4. **Kwang-Jow Gan**, Kuan-Yu Chun, and Dong-Shong Liang, "Frequency Divider Design Using Negative Differential Resistance Circuit", *2010 Australian Communications Theory Workshop*, Canberra, Australian, Feb. 3-5, **2010**.
5. W.K. Yeh, C. C. Wang, C. W. Hsu, Y.K. Fang, S. M. We, C. C. Ou, C. L. Lin, **K. J. Gan**, C. J. Weng, P. Y. Chen, J. S. Yuan, and J. J. Liou, "Impact of Oxide Trap Charge on Performance of Strained Fully Depleted SOI Metal-Gate MOSFET", 2009 IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC 2009), Xian, China, Nov. 25-27, 2009, pp. 197-200.
6. Chih-Hsiang Chang, **Kwang-Jow Gan**, Chun-Liang Lin, and Jeng-Jong Lu, "The Thermal Dissipation Study of Carbon Nanotubes used in High Power LED" *2009 International Conference on Materials for Advanced Technologies*, Singapore, Jun. 28-Jul. 3, 2009, A00998-02186. (ISBN: 978-981-08-3380-0)
7. Dong-Shong Liang, **Kwang-Jow Gan***, Jenq-Jong Lu, Cheng-Chi Tai, Cher-Shiung Tsai, Geng-Huang Lan, and Yaw-Hwang Chen, "Multiple-Valued Memory Design by Standard BiCMOS Technique", *2009 World Congress on Computer Science and Information Engineering*, Los Angeles, California, USA, Mar. 31-Apr. 2, 2009, pp.596~599. (ISBN: 978-0-7695-3507-4)
8. **Kwang-Jow Gan**, Dong-Shong Liang, Cher-Shiung Tsai, Yaw-Hwang Chen, and Cheng-Chi Tai, "Frequency Divider Design Using the Combination of Transistors and Passive Devices", *2009 13th International Symposium on Antenna Technology and Applied Electromagnetics and the Canadian Radio Sciences Meeting*, Banff conference centre, Banff, AB, Canada, February 15 - 18, 2009. (ISBN: 978-1-4244-2980-6)
9. Dong-Shong Liang, Cheng-Chi Tai, and **Kwang-Jow Gan**, "Analysis of Frequency Divider Using Negative Differential Resistance Circuit", *2008 The IASTED International Conference on Circuits and Systems*, Kailua-Kona, Hawaii, USA, Aug 18-20, 2008, pp.93~96. (ISBN:978-0-88986-754-3)

10. Dong-Shong Liang, Cheng-Chi Tai, **Kwang-Jow Gan**, Yi-Zhi Lin, “Selectively Multiple-Valued Memory Design Using Negative Differential Resistance Circuits Implemented by Standard SiGe Bi CMOS Process”, *2008 International Conference on Communications, Circuits and Systems*, Xiamen China, May 25-27, 2008, pp.1208~1211. (ISBN:978-1-4244-2063-6)
11. Dong-Shong Liang, and **Kwang-Jow Gan**, “New D-Type Flip-Flop Design Using Negative Differential Resistance Circuits”, *4th IEEE International Symposium on Electronic Design, Test & Applications (2008 DELTA)*, Hong Kong, China, January 22-25, pp. 258-261, 2008. (ISBN:1-4244-0637-4)
12. Cher-Shiung Tsai, Ming-Hsin Lin, Chien-Hua Chang, Shu-Yin Jiang, Ming-Yuan Guo, **Kwang-Jow Gan**, Dong-Shong Liang, Pei-Hua Chang, and Yaw-Hwang Chen “Wide Band Oscillator Design Based on Bi-CMOS Active Load Differential Amplifier”, *2007 IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC 2007)*, Tainan, Tayih Landis Hotel, Taiwan, ROC., December 20-22, 2007. Vol.2, pp.773-776. (ISBN:1-4244-0637-4)
13. Cher-Shiung Tsai, Ming-Yuan Guo, Chien-Hua Chang, Shu-Yin Jiang, Ming-Hsin Lin, **Kwang-Jow Gan**, Pei-Hua Chang, Dong-Shong Liang and Yaw-Hwang Chen,” A VHF Oscillator Design Based on BJT Active Load Differential Amplifier”, *2007 IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC 2007)*, Tainan, Tayih Landis Hotel, Taiwan, ROC., December 20-22, 2007. Vol.2, pp.917-920. (ISBN:1-4244-0637-4)
14. **Kwang-Jow Gan**, Yi-Jhih Lin, Yaw-Hwang Chen, Cher-Shiung Tsai, and Pei-Hua Chang, “Design of NDR-Based Multiple-Valued Multiplexer Using Standard SiGe Process”, *2007 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Tainan, Tayih Landis Hotel, Taiwan, R.O.C., Dec. 20-22, 2007, Vol.2, pp.925-928. (ISBN:1-4244-0637-4)
15. **Kwang-Jow Gan***, Dong-Shong Liang, Cher-Shiung Tsai, Chun-Ming Wen, Yi-Zhi Lin, and Te-Chia Chang, “Design of Four-Valued Memory Using Three-Peak MOS-HBT-NDR Circuits”, *The Fifth IASTED International Conference on Circuits, Signals, and Systems*, Banff, Alberta, Canada, July 2-4, 2007, No. 573-022 (ISBN:978-0-88986-670-6)
16. **Kwang-Jow Gan***, Dong-Shong Liang, Cher-Shiung Tsai, Yi-Jhih Lin, Yaw-Hwang Chen, Te-Chia Chang, and Wein-So Wang, “Novel Multiple-Valued Memory Design by Standard SiGe Process”, *4th International Conference on Materials for Advanced Technologies (ICMAT 2007)*, Singapore July 1-6, 2007, pp. 46, (ISBN:978-81-904438-0-7).
17. Dong-Shong Liang, **Kwang-Jow Gan***, Cher-Shiung Tsai, Te-Chia Chang, and Yi-Jhih Lin “New Negative Differential Resistance Device Design Suitable for

- Standard SiGe BiCMOS Nano-Technique”, *4th International Conference on Materials for Advanced Technologies (ICMAT 2007)*, Singapore July 1-6, 2007, pp. 46, (ISBN: 978-81-904438-0-7).
18. **Kwang-Jow Gan***, Dong-Shong Liang, Cher-Shiung Tsai, Yaw-Hwang Chen, and Chun-Ming Wen, “Five-State Logic Using MOS-HBT-NDR Circuit by Standard SiGe BiCMOS Process”, *2006 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2006)*, Singapore Dec. 4-7, 2006, pp. 1356-1359. (ISBN:1-4244-0387-1).
 19. Dong-Shong Liang, **Kwang-Jow Gan***, Cher-Shiung Tsai, and Yaw-Hwang Chen, “AND and NAND Logic Circuit Design Using NDR-Based Device Suitable for CMOS Process”, *2006 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2006)*, Singapore Dec. 4-7, 2006, pp. 1360-1363. (ISBN:1-4244-0387-1).
 20. Dong-Shong Liang, Yaw-Hwang Chen, Chun-Min Wen, Chun-Da Tu, **Kwang-Jow Gan** and Cher-Shiung Tsai, “The Design of MOS-NDR-Based Cellular Neural Network”, *2006 International Joint Conference on Neural Networks*, Sheraton Vancouver Wall Centre, Vancouver, BC, Canada, July 16-21, 2006, pp.2012-2014. (ISBN:0-7803-9490-9).
 21. Dong-Shong Liang, **Kwang-Jow Gan***, Chun-Da Tu, Cher-Shiung Tsai, and Yaw-Hwang Chen, “Frequency Multiplier Design Based on Multiple-Peak R-BJT-NDR Devices Fabricated by SiGe Technology”, *16th Biennial University Government Industry Microelectronics Symposium*, San Jose State University, San Jose, CA, USA, June 25-28, 2006, pp. 239-242. (ISBN:1-4244-0268-9).
 22. Dong-Shong Liang, Yaw-Hwang Chen, Chun-Min Wen, Chun-Da Tu, **Kwang-Jow Gan**, and Cher-Shiung Tsai, “The Design of MOS-BJT-NDR-Based Cellular Neural Network”, *16th Biennial University Government Industry Microelectronics Symposium*, San Jose State University, San Jose, CA, USA, June 25-28, 2006, pp. 187-188. (ISBN:1-4244-0268-9).
 23. **Kwang-Jow Gan***, Dong-Shong Liang, Cher-Shiung Tsai, Yaw-Hwang Chen, and Shin-Bin Kuo, “OR and NOR Logic Circuit Design Using Negative Differential Resistance Device Fabricated by CMOS Process”, *2005 IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC)*, New World Renaissance Hotel, Hong Kong, China, Dec. 19-21, 2005, pp. 813-816. (ISBN:0-7803-9339-2).
 24. **Kwang-Jow Gan***, Dong-Shong Liang, Chung-Chih Hsiao, Cher-Shiung Tsai, and Yaw-Hwang Chen, “Investigation of MOS-NDR Voltage Controlled Ring Oscillator Fabricated by CMOS Process”, *2005 IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC)*, New World Renaissance Hotel,

- Hong Kong, China, Dec. 19-21, 2005, pp. 825-827. (ISBN:0-7803-9339-2).
25. **Kwang-Jow Gan***, Dong-Shong Liang, Chung-Chih Hsiao, Shih-Yu Wang, Feng-Chang Chiang, Cher-Shiung Tsai, Yaw-Hwang Chen, Shun-Huo Kuo, and Chi-Pin Chen, "Logic Circuit Design Based on MOS-NDR Devices and Circuits Fabricated by CMOS Process", *2005 International Workshop on System-on-Chip*, Banff, Alberta, Canada, July 20-24, 2005, pp. 392-395. (ISBN:0-7695-2403-6).
 26. Dong-Shong Liang, **Kwang-Jow Gan***, Chung-Chih Hsiao, Cher-Shiung Tsai, Yaw-Hwang Chen, Shih-Yu Wang, Shun-Huo Kuo, Feng-Chang Chiang, and Long-Xian Su, "Novel Voltage-Controlled Oscillator Design by MOS-NDR Devices and Circuits", *2005 International Workshop on System-on-Chip*, Banff, Alberta, Canada, July 20-24, 2005, pp. 372-375. (ISBN:0-7695-2403-6).
 27. Dong-Shong Liang, **Kwang-Jow Gan***, Long-Xian Su, Chi-Pin Chen, Chung-Chih Hsiao, Cher-Shiung Tsai, Yaw-Hwang Chen, Shih-Yu Wang, Shun-Huo Kuo, and Feng-Chang Chiang, "Four-Valued Memory Circuit Designed by Multiple-Peak MOS-NDR Devices and Circuits", *2005 International Workshop on System-on-Chip*, Banff, Alberta, Canada, July 20-24, 2005, pp. 78-81. (ISBN:0-7695-2403-6).
 28. **Kwang-Jow Gan***, Dong-Shong Liang, Shih-Yu Wang, Chung-Chih Hsiao, Cher-Shiung Tsai, Yaw-Hwang Chen, and Feng-Chang Chiang, "High-Frequency Voltage-Controlled Oscillator Design by MOS-MDR Devices and Circuits", *2005 IEEE AP-S Interational Symposium and USNC/URSI National Radio Science Meeting*, Omni Shoreham Hotel, NW, Washington, DC, USA, July 3-8, 2005, pp. 33. (ISBN:0-7803-8884-4).
 29. T. S. Wu, Y. K. Su, F. S. Juang, N. Y. Li, and **K. J. Gan**, "Ohmic and Schottky contacts to GaSb," *International Conference on Thin Film and Applications*, Shanghai, China, pp. 15-17, April, 1991.
 30. T. S. Wu, Y. K. Su, F. S. Juang, N. Y. Li, and **K. J. Gan**, "Effects of TMSb/TEGa ratios on epilayer properties of GaSb grown by low pressure MOCVD, " *SPIE's International Conference on Physical Concepts for Novel Optoelectronic Device Applications*, Aachen, Federal Republic of Germany. 1990.

III. International Conference (local)

1. B.-J. Li, C.-H Chang, Y.-K. Su, **K.-J. Gan**, and J.-W. Hong," Application of Multi-Wall Carbon Nanotube/SiC Composite to Thermal Dissipation of High-Bright Light Emitting Diode", *International Symposium on*

- Next-Generation Electronics (ISNE), National Sun Yat-Sen University, Kaohsiung, Taiwan, Nov. 18-19, 2010.
2. Cher-Shiung Tsai, Ming-Hsin Lin, Ping-Feng Wu, Wu-Yan Sie, Yu-Nan Yeh, Chang-Yu Li, Wei-cheng Liu, Hsiang-Tse Cheng, Chun-Yi Yeh, **Kwang-Jow Gan**, Pei-Hua Chang, and Chia-Hsiang Chang, "An Oscillator Design Based on Bi-CMOS Cascoded Active Load Differential Amplifier Using Standard 0.35 μ m SiGe Process", *2009 National Symposium on Telecommunications*, National University of Kaohsiung, December 11-12, 2009, pp. 138-141.
 3. J. S. Chang, **K. J. Gan**, C. L. Lin, and J. J. Lu, "Investigation catalyst of the growth quality for carbon nanotube", *2008 IEEE International Workshop on Next Generation Electronics (IWNE)*, Kun Shan University, Tainan County, Taiwan, November 20-21, 2008, pp. 119-120. (ISBN:978-986-6507-04-5)
 4. J. L. Hsu, C. C. Lin, **K. J. Gan**, and S. Y. Tsai, "Microstructural and surface morphology of GZO films deposited by sputtering", *2008 IEEE International Workshop on Next Generation Electronics (IWNE)*, Kun Shan University, Tainan County, Taiwan, November 20-21, 2008, pp. 87-88. (ISBN:978-986-6507-04-5)
 5. G. H. Lan, **K. J. Gan**, C. S. Tsai, P. H. Chang, D. S. Liang and Y. H. Chen, "Multiple-Valued Memory Cell Design Based on Lamda Type MOS-HBT-NDR Circuits", *2008 IEEE International Workshop on Next Generation Electronics (IWNE)*, Kun Shan University, Tainan County, Taiwan, November 20-21, 2008, pp. 23-24. (ISBN:978-986-6507-04-5)
 6. Y. K. LI, **K. J. Gan**, C. S. Tsai, P. H. Chang and Y. H. Chen, "Achieve a New Type Frequency Divider Circuit and Application By MOS-HBT-NDR", *2008 IEEE International Workshop on Next Generation Electronics (IWNE)*, Kun Shan University, Tainan County, Taiwan, November 20-21, 2008, pp. 25-26. (ISBN:978-986-6507-04-5)
 7. Y. W. Chen, **K. J. Gan**, C. S. Tsai, D. S. Liang and Y. H. Chen, "Analysis of Multi-Peak Memory Circuit Using Resistor as Load", *2008 IEEE International Workshop on Next Generation Electronics (IWNE)*, Kun Shan University, Tainan County, Taiwan, November 20-21, 2008, pp. 27-28. (ISBN:978-986-6507-04-5)
 8. Cher-Shiung Tsai, Ming-Hsin Lin, Ping-Feng Wu, Chang-Yu Li, Yu-Nan Yeh, Wu-Yan Sie, **Kwang-Jow Gan**, Pei-Hua Chang, Dong-Shong Liang, Jin-Wei Wu and Chia-Hsiang Chang, "An Oscillator Design Based on Bi-CMOS Differential Amplifier Using Standard SiGe Process", *2008 IEEE International Workshop on Next Generation Electronics (IWNE)*, Kun Shan University, Tainan County, Taiwan, November 20-21, 2008, pp. 45-46.

(ISBN:978-986-6507-04-5)

9. **Kwang-Jow Gan**, Te-Chia Chang, Cheng-Syuan Wang, Cher-Shiung Tsai, Yaw-Hwang Chen, Wein-So Wang, “Frequency Divider Design Using Novel BiCMOS-Based Negative Differential Resistance Circuit” , *2008 Asia-Pacific Chinese Conference on High-Speed Circuit Design (HSCD'08)*, St. John's University, Taipei, Taiwan, R.O.C., July 22-23, 2008. (ISBN:986-6765-07-5)
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Projects

A. National Science Council Projects

1. Fabrication of carbon nanotube and Its application to the thermal dissipation of high-brightness ◦ (NSC98-2221-E-415-017 , **2009/08~2010/07**) ◦
2. Lamp designs using white-light light emitting diode focusing on illumination ◦ (NSC97-2623-E-168-001-IT , **2008/10~2009/09**) ◦
3. Novel applications using multiple-valued negative differential resistance circuit suitable for BiCMOS process (II) ◦ (NSC97-2221-E-168-045 , **2008/08~2009/07**) ◦
4. Fabrication of wide-band voltage-controlled oscillator using differential amplifier ◦ (NSC97-2221-E-168-046 , **2008/08~2009/07**) ◦
5. Novel applications using multiple-valued negative differential resistance circuit suitable for BiCMOS process (I) ◦ (NSC96-2221-E-168-033 , **2007/08~2008/07**) ◦
6. Development of new-type MOS-BJT-NDR devices and applied integrated circuits (3/3) ◦ (NSC95-2221-E-168-037 , **2006/08~2007/07**) ◦
7. Development of new-type MOS-BJT-NDR devices and applied integrated circuits (2/3) ◦ (NSC94-2215-E-168-001 , **2005/08~2006/07**) ◦
8. High-frequency voltage-controlled oscillator using negative differential resistance device ◦ (NSC94-2815-C-168-005-E , **2005/07~2006/02**) ◦
9. Development of new-type MOS-BJT-NDR devices and applied integrated circuits (1/3) ◦ (NSC93-2215-E-168-002 , **2004/08~2005/07**) ◦
10. Design and fabrication of high-adjustment negative differential resistance devices and applied integrated circuits ◦ (NSC92-2218-E-168-005 , **2003/08~2004/07**) ◦
11. Research of negative differential resistance devices and applied integrated circuits suitable for CMOS and BiCMOS processes ◦ (NSC91-2215-E-168-001 , **2002/08~2003/07**) ◦
12. Design and S-type and N-type negative differential resistance devices using transistors and their applications ◦ (NSC90-2215-E-168-002 , **2001/08~2002/07**) ◦
13. Negative-differential-resistance devices, designs and applications introduced by interactive computer aided simulation and teaching system ◦ (NSC90-2516-S-168-001 , **2001/08~2002/07**) ◦
14. Computer aided design - Research of the current-voltage characteristics, hysteresis phenomena, and applications using the series-connected Esaki-like N-type negative differential resistance devices ◦ (NSC89-2215-E-168-005 , **2000/08~2001/07**) ◦
15. Computer aided design - Research of the combined current-voltage characteristics of the series-connected negative differential resistance devices ◦ (NSC89-2215-E-168-003 , **1999/08~2000/07**) ◦

B. General Projects

1. Design of multi-function LED light modulation module ◦ **(2010/04~2011/1)**
2. Lamp designs using white-light light emitting diode focusing on illumination ◦ **(2008/10~2011/9)**
3. Fabrication of transparent electrodes for applying to Nitride-based light emitting diode ◦ **(2008/01~2008/12)**
4. Fabrication of nano-based high-efficient waterproof cardboard ◦ **(2008/06~2009/1)** ◦
5. Advanced project for the nanotechnology talent in college ◦ **(2008/05~2008/12)** ◦
6. Advanced project for the nanotechnology talent in college ◦ **(2007/05~2007/12)** ◦
7. Development of the advanced nano materials ◦ **(2006/08~2007/07)** ◦
8. Advanced project for the nanotechnology talent in college ◦ **(2006/05~2006/12)** ◦